FIG. 2(b) is a timing chart showing an output voltage of the power switch, and FIG. 2(c) is a timing chart showing an ON current flowing through the power switch;

[0029] FIG. 3(a) is a circuit block diagram showing a soft-start charge pump circuit according to the present invention applied to drive a power switch;

[0030] FIG. 3(b) is a waveform timing chart showing an example of amplitude modulating clock signals according to the present invention;

[0031] FIG. 4(a) is a circuit block diagram showing a clock amplitude modulator according to the present invention;

[0032] FIG. 4(b) is a detailed circuit diagram showing an example of a clock amplitude modulator according to the present invention;

[0033] FIGs. 5(a) to 5(d) are operational timing charts showing a soft-start charge pump circuit according to the present invention applied to drive a power switch, wherein FIG. 5(a) is a timing chart showing a soft-start control signal output from a soft-start controller, FIG. 5(b) is a timing chart showing a soft-start pumping voltage generated by the soft-start charge pump circuit, FIG. 5(c) is a timing chart showing an output voltage of the power switch, and FIG. 5(d) is a timing chart showing an ON current flowing